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PATENT

FREQUENCY SYNTHESIZER USING DIGITAL
PRE-DISTORTION AND METHOD

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit under 35 U.S.C. § 119(e) of U.S. Patent Application Serial No. 60/458,515 filed on March 28, 2003.

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TECHNICAL FIELD

[0002] This disclosure is generally directed to communication systems and more specifically to a frequency synthesizer using digital pre-distortion and method.

BACKGROUND

[0003] Wireless communication devices typically include a frequency synthesizer, which is often a critical component of many techniques used to modulate data onto an outgoing wireless
5 signal. Conventional modulation techniques, such as Gaussian Frequency Shift Keyed (GFSK) modulation, are typically implemented using either I-Q up-conversion or by direct open-loop modulation of a voltage-controlled oscillator (VCO). The up-conversion approach is often susceptible to an undesired image
10 signal and is typically costly in terms of analog area and power. The open-loop modulation approach is often prone to frequency drift in the voltage-controlled oscillator and to gain errors.

SUMMARY

[0004] This disclosure provides a frequency synthesizer using digital pre-distortion and method.

[0005] In one aspect, a method includes identifying a setting
5 for a capacitor bank associated with a voltage-controlled oscillator in a closed-loop phase-locked-loop. The setting represents a combination of one or more capacitors in the capacitor bank. The method also includes estimating a gain introduced by the closed-loop phase-locked-loop when the
10 oscillator operates using the identified setting. The method further includes estimating a response of a loop filter in the phase-locked-loop and identifying one or more coefficients for a digital filter using the identified gain and the identified loop filter response. The digital filter is operable to filter an
15 input signal. In addition, the method includes modulating the filtered input signal using the phase-locked-loop to produce an output signal.

[0006] One or more technical features may be present according to various embodiments of this disclosure. Particular
20 embodiments of this disclosure may exhibit none, some, or all of the following features depending on the implementation. For example, in one embodiment, a frequency synthesizer using digital pre-distortion is provided. In particular, the frequency

synthesizer uses closed-loop modulation of a phase-locked-loop to produce an output signal. The use of closed-loop modulation may introduce various irregularities in the output signal. As examples, the output signal may suffer from loop gain in the phase-locked-loop and from variations in a loop filter used in the phase-locked-loop.

[0007] To at least partially compensate for the various irregularities in the output signal, the frequency synthesizer also includes a digital pre-distortion filter. The pre-distortion filter distorts an input signal before it is modulated by the phase-locked-loop to produce the output signal. This distortion changes the input signal in such a way as to at least partially correct for the irregularities introduced by the phase-locked-loop. As a result, the output signal produced may have fewer or no irregularities. In a particular embodiment, the pre-distortion filter distorts the input signal such that the output signal is compliant with the Bluetooth standard.

[0008] This has outlined rather broadly several features of this disclosure so that those skilled in the art may better understand the DETAILED DESCRIPTION that follows. Additional features may be described later in this document. Those skilled in the art should appreciate that they may readily use the concepts and the specific embodiments disclosed as a basis for

modifying or designing other structures for carrying out the same purposes of this disclosure. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

5 [0009] Before undertaking the DETAILED DESCRIPTION below, it may be advantageous to set forth definitions of certain words and phrases used throughout this patent document. The terms "include" and "comprise," as well as derivatives thereof, mean inclusion without limitation. The term "or" is inclusive,
10 meaning and/or. The phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean to include, be included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be
15 bound to or with, have, have a property of, or the like. The term "controller" means any device, system, or part thereof that controls at least one operation. A controller may be implemented in hardware, firmware, or software, or a combination of at least two of the same. It should be noted that the functionality
20 associated with any particular controller may be centralized or distributed, whether locally or remotely. Definitions for certain words and phrases are provided throughout this patent document, and those of ordinary skill in the art should

understand that in many, if not most instances, such definitions apply to prior as well as future uses of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] For a more complete understanding of this disclosure and its features, reference is now made to the following description taken in conjunction with the accompanying drawings, in which:

[0011] FIGURE 1 illustrates an example wireless device according to one embodiment of this disclosure;

[0012] FIGURE 2 illustrates an example frequency synthesizer according to one embodiment of this disclosure;

10 [0013] FIGURE 3 illustrates an example capacitor selection circuit according to one embodiment of this disclosure;

[0014] FIGURE 4 illustrates an example gain calibration circuit according to one embodiment of this disclosure; and

[0015] FIGURE 5 illustrates an example method for digital pre-
15 distortion according to one embodiment of this disclosure.

DETAILED DESCRIPTION

[0016] FIGURE 1 illustrates an example wireless device 100 according to one embodiment of this disclosure. The wireless device 100 illustrated in FIGURE 1 is for illustration only.

5 Other wireless devices could be used without departing from the scope of this disclosure. Also, the wireless device 100 in FIGURE 1 has been simplified for ease of illustration and explanation. Other or additional components could be included in the wireless device 100.

10 [0017] In the illustrated embodiment, the wireless device 100 includes an antenna 102. The antenna 102 facilitates the communication of information over a wireless interface. The antenna 102 may represent any suitable structure that is operable to facilitate the transmission or reception of wireless signals.

15 As a particular example, the antenna 102 may support the transmission and reception of radio frequency signals.

[0018] Radio frequency (RF) processing circuitry 103 is coupled to the antenna 102. In this document, the term "couple" refers to any direct or indirect communication between two or

20 more components, whether or not those components are in physical contact with one another. The RF processing circuitry 103 processes the signals transmitted or received by the antenna 102. As particular examples, the RF processing circuitry 103 could

include one or more low-noise amplifiers, mixers, filters, and power amplifiers.

[0019] A transceiver 104 is coupled to the RF processing circuitry 103. The transceiver 104 may receive an incoming
5 signal received by the antenna 102 and down-convert the signal to generate a baseband or intermediate frequency signal. The transceiver 104 may also receive a baseband signal or an intermediate frequency signal and up-convert the signal for transmission by the antenna 102. The transceiver 104 could
10 include any hardware, software, firmware, or combination thereof for facilitating communication using the antenna 102. As a particular example, the transceiver 104 could include a transmitter and a receiver.

[0020] Receive circuitry 106 is coupled to the transceiver
15 104. The receive circuitry 106 receives and processes incoming signals received by the wireless device 100. For example, the receive circuitry 106 may receive the baseband or intermediate frequency signal produced by the transceiver 104 and process the signal to extract information contained in the signal. The
20 receive circuitry 106 may include any hardware, software, firmware, or combination thereof for processing incoming signals, such as a filter or decoder. In the illustrated example, the incoming signal represents voice information; and the extracted

voice information may be provided to a speaker 108 for presentation to a user.

[0021] Transmit circuitry 110 is coupled to the transceiver 104. The transmit circuitry 110 receives and processes outgoing
5 signals for transmission by the wireless device 100. For example, the transmit circuitry 110 may receive voice information and process the information to produce a baseband or intermediate frequency signal. The baseband or intermediate frequency signal may then be provided to the transceiver 104. The transmit
10 circuitry 110 may include any hardware, software, firmware, or combination thereof for processing outgoing signals, such as a filter or an encoder. In the illustrated example, the outgoing signal may include voice information collected by a microphone 112.

15 [0022] A controller 114 is connected to the receive circuitry 106 and the transmit circuitry 110. The controller 114 controls the operation and behavior of the wireless device 100. For example, the controller 114 could allow a user to mute the wireless device 100 so that no voice information is transmitted
20 by the wireless device 100. In this example, the controller 114 may instruct the transmit circuitry 110 to stop transmitting information when the wireless device 100 is muted. The controller 114 could represent any suitable controller, such as a

processor. The logic executed by the controller 114 could be stored in a memory 116, which may represent any suitable storage and retrieval device or devices. In other embodiments, the controller 114 and the memory 116 could be omitted from the
5 wireless device 100.

[0023] In one aspect of operation, the wireless device 100 may include a frequency synthesizer, such as a frequency synthesizer 118 in the transceiver 104. The frequency synthesizer 118 uses closed-loop modulation of a phase-locked-loop (PLL) to produce a
10 phase or frequency modulated output signal, such as the outgoing signal transmitted by the antenna 102. The use of closed-loop modulation may introduce various irregularities in the output signal. To at least partially compensate for the various irregularities in the output signal, the frequency synthesizer
15 118 includes a digital pre-distortion filter, which distorts an input signal before it is modulated by the phase-locked-loop to produce the output signal. This distortion changes the input signal in a way that at least partially corrects for the irregularities introduced by the phase-locked-loop. As a result,
20 the phase-locked-loop may produce an output signal having fewer or no irregularities.

[0024] This frequency synthesizer 118 could be used in any suitable wireless device 100. For example, the wireless device

100 could represent a Bluetooth device, a Digital Enhanced Cordless Telephone (DECT) device, or a Global System for Mobile communication (GSM) device. In the example shown in FIGURE 1, the wireless device 100 could represent a mobile headset that may
5 be worn by a user and that facilitates the communication of voice information to and from a mobile or other telephone. The wireless device 100 could also represent a mobile handset, a base station, or any other suitable device. The frequency synthesizer 118 could also support any suitable modulation technique,
10 including Frequency Shift Keyed (FSK) modulation, Gaussian Frequency Shift Keyed (GFSK) modulation, or Gaussian Minimum Shift Keyed (GMSK) modulation.

[0025] Although FIGURE 1 illustrates one example of a wireless device 100, various changes may be made to FIGURE 1. For
15 example, other one-way or multi-way communication devices could be used. As a particular example, FIGURE 1 illustrates a wireless device 100 providing voice services. Other devices, such as devices connecting a computer to a printer or to a personal digital assistant, could use the frequency synthesizer
20 118. Also, various components could be combined or omitted or additional components can be added to the wireless device 100 according to particular needs. In addition, the transceiver 104

could be replaced by a transmitter, and the receive circuitry 106 could be omitted in the wireless device 100.

[0026] FIGURE 2 illustrates an example frequency synthesizer 200 according to one embodiment of this disclosure. The frequency synthesizer 200 illustrated in FIGURE 2 may, for example, be used as the frequency synthesizer 118 in the wireless device 100 of FIGURE 1. The frequency synthesizer 200 shown in FIGURE 2 is for illustration only. Other embodiments of the frequency synthesizer 200 could be used without departing from the scope of this disclosure.

[0027] The frequency synthesizer 200 is operable to receive an input signal (f_{in}) 202 and produce an output signal (f_{out}) 204, where f_{in} represents a desired value for the instantaneous output frequency and f_{out} is the actual instantaneous output frequency. In the illustrated example, the frequency synthesizer 200 includes a phase-locked-loop 206. The phase-locked-loop 206 is used to produce the output signal 204 by modulating the input signal 202. In a particular embodiment, a Bluetooth-compliant wireless device 100 can transmit or receive GFSK modulated data on one of eighty 1MHz channels spanning 2.402-2.480 GHz. In this embodiment, the frequency synthesizer 200 pre-distorts the input signal 202 before it is modulated, and the pre-distortion alters

the input signal 202 so the output signal 204 is compliant with the Bluetooth standard.

[0028] In this example, the phase-locked-loop 206 includes a phase detector/charge pump (PD/CP) 208. The phase detector 208
5 identifies a phase difference between a reference signal (f_{ref}) 210 and a signal provided by a frequency divider 216. The phase detector/charge pump 208 outputs a signal proportional to this phase difference.

[0029] A loop filter 212 is coupled to the phase detector/
10 charge pump 208. The loop filter 212 filters the signal generated by the phase detector/charge pump 208. The loop filter 212 may represent any suitable filter, such as a low-pass filter or a band-pass filter. In other embodiments, the loop filter 208 could be omitted from the frequency synthesizer 200.

[0030] A voltage-controlled oscillator (VCO) 214 is coupled to
15 the loop filter 212. The oscillator 214 is operable to produce the output signal 204. In one embodiment, the frequency of the signal produced by the oscillator 214 is controlled by the signal produced by the phase detector/charge pump 208 and filtered by
20 the loop filter 212. The oscillator 214 may include any suitable oscillator operable to generate the output signal 204.

[0031] In one embodiment, the oscillator 214 includes a capacitor bank that has selectable capacitors. In this

embodiment, the frequency of the output signal 204 generated by the oscillator 214 can be at least partially controlled by selecting various combinations of capacitors in the capacitor bank. In a particular embodiment, the capacitor bank in the oscillator 214 includes 64 different settings corresponding to a range of approximately 500 MHz with approximately 8 MHz per setting.

[0032] A frequency divider 216 is coupled to the oscillator 214 and to the phase detector/charge pump 208. The divider 216 is operable to alter the frequency of the output signal 204 produced by the oscillator 214. The divider 216 then provides the altered output signal to the phase detector/charge pump 208.

By controlling how the divider 216 alters the frequency of the output signal 204, the behavior of the phase-locked-loop 206 can be controlled.

[0033] A modulator 218 is coupled to the divider 216. The modulator 218 is operable to receive and modulate the input signal 202. The resulting modulated signal is provided to the divider 216, which uses the modulated signal to alter the output signal 204 generated by the oscillator 214. In this way, the modulator 218 controls the operation of the divider 216, which allows the modulator 218 to control the operation of the phase-

locked-loop 206. The modulator 218 may represent any suitable modulator, such as a Delta-Sigma ($\Delta\Sigma$) modulator.

[0034] The frequency synthesizer 200 also includes a digital filter 220. The digital filter 220 performs data filtering on the input signal 202 before the input signal is modulated by the phase-locked-loop 206. The digital filter 220 may represent any suitable digital filter. In a particular embodiment, the digital filter 220 represents a digital Gaussian filter that performs filtering for the Bluetooth standard.

[0035] The phase-locked-loop 206 shown in FIGURE 2 represents a closed-loop modulator, which may introduce various irregularities into the output signal 204. For example, the phase-locked-loop 206 may introduce gain into the output signal 204. Also, variations in the loop filter 212 may alter the output signal 204 in undesired ways. Further, due to noise considerations, it may be difficult to implement a closed-loop phase-locked-loop 206 with a wide enough loop bandwidth to modulate data directly. As a particular example, the phase-locked-loop 206 may have a loop bandwidth of 100 kHz and a data modulation bandwidth of greater than 100 kHz. If left uncompensated, the response of this phase-locked-loop 206 could cause unwanted low-pass filtering of the input signal 202.

[0036] To help compensate for these or other irregularities, a pre-distortion filter 222 is provided in the frequency synthesizer 200. The digital pre-distortion filter 222 is coupled to the digital filter 220 and the modulator 218. As described below, the digital pre-distortion filter 222 is inserted in the data signal path to cancel the response of the phase-locked-loop 206. In effect, the digital pre-distortion filter 222 alters the input signal 202 so that the variations produced by the phase-locked-loop 206 are at least partially reduced or eliminated. The digital pre-distortion filter 222 may represent any suitable digital filter. In one embodiment, the digital pre-distortion filter 222 includes adjustable coefficients, which may be altered to change the behavior of the digital pre-distortion filter 222.

[0037] As described below, various functions may be performed to control the operation of the frequency synthesizer 200. This may include the execution of a tuning algorithm that controls the selection of capacitors in the capacitor bank of the voltage-controlled oscillator 214. This may also include an algorithm for estimating the loop gain of the phase-locked-loop 206 and an algorithm for estimating the response of the loop filter 212. In addition, this may include an algorithm for calculating the coefficient settings of the pre-distortion filter 222. In one

embodiment, some or all of these algorithms could represent on-chip algorithms. In one embodiment, the frequency synthesizer 200 includes a controller 224 that executes the algorithms and a memory 226 that stores the algorithms. Other embodiments of the frequency synthesizer 200 could also be used.

[0038] In a particular embodiment, the frequency synthesizer 200 supports the Bluetooth standard. The Bluetooth standard represents a frequency hopping system, where receive-to-transmit turnaround time is 220 μ s, and the settling time of the frequency synthesizer 200 is less than that when software and baseband overhead is considered. The various algorithms described above may be executed each time a frequency hop is performed, which helps to account for:

(1) different capacitor select settings in the capacitor bank of the oscillator 214 over process, temperature, and the Bluetooth frequency range;

(2) different gains (and hence different loop gains) over process, temperature, and the Bluetooth frequency range; and

(3) different component values in the loop filter 212 over process and temperature.

For many wireless communication systems, the time spent on one transmission may be relatively short. Thus, for a given transmission, the temperature variation may be small, so the

capacitor selection, gain calibration, and loop filter calibration could be essentially static.

[0039] Although FIGURE 2 illustrates one example of a frequency synthesizer 200, various changes may be made to FIGURE 2. For example, the loop filter 212 may be removed from the frequency synthesizer 200. Also, the digital filter 220 and the digital pre-distortion filter 222 could be combined into a single filter.

[0040] FIGURE 3 illustrates an example capacitor selection circuit 300 according to one embodiment of this disclosure. The capacitor selection circuit 300 may, for example, be used in the frequency synthesizer 200 of FIGURE 2 to select the capacitors used in the capacitor bank of the voltage-controlled oscillator 214. Other embodiments of the capacitor selection circuit 300 may be used without departing from the scope of this disclosure.

[0041] In the illustrated example, the frequency synthesizer 200 is configured as a digital frequency-locked loop. In this example, the frequency of the signal produced by the voltage-controlled oscillator 214 is controlled by selecting various combinations of capacitors in a capacitor bank. Each combination of capacitors may correspond to a different setting. In a particular embodiment, the capacitor bank includes 64 different settings, which can be represented by a six-bit value.

[0042] The frequency synthesizer 200 may execute a capacitor selection algorithm to select a setting for the capacitor bank in the oscillator 214. During the execution of this algorithm, the oscillator 214 receives a common mode voltage (VCM) 302. In this
5 embodiment, the input to the voltage-controlled oscillator (VCO) 214 is forced to the common mode voltage 302, and the VCO 214 is in the center of its analog tuning range. In other embodiments, a different voltage input to the VCO 214 may be appropriate.

[0043] The signal produced by the oscillator 214 is supplied
10 to a prescaler 304. The prescaler 304 receives and divides the signal from the oscillator 214. For example, the prescaler 304 may divide the signal produced by the oscillator 214 by eight. In effect, this decreases the frequency of the signal produced by the oscillator 214 by a factor of eight. The prescaler 304 may
15 represent any suitable structure that can divide the frequency of a signal.

[0044] The prescaler 304 supplies the divided signal to a counter 306. The counter 306 is clocked by the prescaler 304 to produce an output counter signal. The counter 306 could
20 represent any suitable counter, such as an M counter. The output signal from the counter 306 is supplied to a re-sync unit 308. The re-sync unit 306 synchronizes the output signal of the counter 306 with the digital components of the capacitor

selection circuit 300. The re-sync unit 308 may represent any suitable structure for synchronizing a signal with a digital domain. In other embodiments, other circuits providing a digital estimate of the VCO's instantaneous output could be used.

5 [0045] A digital frequency discriminator 310 estimates the frequency of the signal produced by the counter 306. In one embodiment, the digital frequency discriminator 310 receives the reference signal 210 and counts the number of outputs produced by the counter 306 during each cycle of the reference signal 210.

10 The digital frequency discriminator 310 then outputs an estimated frequency (f_{ESTIMATE}) 312 representing an estimate of the frequency of the counter 306. Because the output of the counter 306 represents a scaled version of the signal output by the oscillator 214, the estimated frequency 312 also represents an

15 estimate of the frequency of the oscillator 214. In a particular embodiment, the signal 312 has a frequency of:

$$f_{\text{ESTIMATE}} = \frac{f_{\text{VCO}}}{8 f_{\text{REF}}}$$

where f_{VCO} represents the frequency of the signal produced by the oscillator 214, and f_{REF} represents the reference frequency 210

20 provided to the frequency synthesizer 200.

[0046] An adder 314 is coupled to the digital frequency discriminator 310. The adder 314 is operable to receive the

estimated frequency 312 produced by the digital frequency discriminator 310 and a desired frequency (f_{DESIRED}) 316 identifying the desired frequency of the signal 312. The adder 314 then subtracts the estimated frequency 312 from the desired frequency 316 to calculate a difference between the frequencies 312, 316. The adder 314 may include any suitable structure operable to identify the difference between two signals. An integrator 318 receives the results of the subtraction performed by the adder 314. The integrator 318 accumulates the differences produced by the adder 314. The integrator 318 may represent any suitable accumulator.

[0047] A low-pass filter 320 is coupled to the integrator 318 and filters the accumulated differences produced by the integrator 318. For example, the low-pass filter 320 may attenuate feedback variation caused by frequency quantization noise. The filtered signals produced by the filter 320 are averaged by an averaging unit 322. The resulting average 324 represents one of the capacitor settings in the capacitor bank of the voltage-controlled oscillator 214.

[0048] In one aspect of operation, the voltage-controlled oscillator 214 contains a bank of selectable capacitors, which allows the frequency of the voltage-controlled oscillator 214 to be coarsely set. A capacitor selection algorithm in the

frequency synthesizer 200 is executed, which configures the frequency synthesizer 200 as a digital frequency-locked loop. For example, the capacitor selection algorithm could cause the oscillator 214 to begin receiving the common mode voltage 302.

5 The capacitor selection algorithm then allows the capacitor selection circuit 300 to operate. The capacitor selection circuit 300 digitally estimates the frequency of the oscillator 214 and chooses the setting of the capacitor bank based on this frequency estimate. The feedback path in the capacitor selection
10 circuit 300 may continuously adjust the capacitor select setting of the oscillator 214 so that the estimated frequency 312 remains equal to or approximately equal to the desired frequency 316. The average capacitor select value 324 produced by the averaging unit 322 may be stored for use during the remainder of a
15 transmission by the frequency synthesizer 200. In one embodiment, this mechanism may be faster than conventional approaches, such as successive-approximation register (SAR) algorithms, because the output of the oscillator 214 may be sampled more often. This may help to reduce frequency
20 quantization error and reduce the time needed for an accurate frequency estimate.

[0049] Although FIGURE 3 illustrates one example of a capacitor selection circuit 300, various changes may be made to

FIGURE 3. For example, other or additional components could be used in the capacitor selection circuit 300.

[0050] FIGURE 4 illustrates an example gain calibration circuit 400 according to one embodiment of this disclosure. The gain calibration circuit 400 may, for example, be used in the frequency synthesizer 200 of FIGURE 2 to identify the gain introduced by the phase-locked-loop 206. Other embodiments of the gain calibration circuit 400 may be used without departing from the scope of this disclosure.

[0051] In the illustrated example, the frequency synthesizer 200 is again configured as a digital frequency-locked loop. In this example, the frequency of the signal produced by the voltage-controlled oscillator 214 is controlled using an adjustable current digital-to-analog converter (DAC) 402 in the charge pump 208 of the phase-locked-loop 206.

[0052] As shown in FIGURE 4, the gain calibration circuit 400 includes the voltage-controlled oscillator 214 of FIGURE 2 and the components 304-322 from the capacitor selection circuit 300 of FIGURE 3. In this embodiment, the average capacitor select value 324 previously produced by the capacitor selection circuit 300 is saved and supplied to the voltage-controlled oscillator 214. A gain calibration algorithm is then executed to estimate the open loop unity gain bandwidth ω_{LOOP} of the phase-locked-loop

206. This information is used to select a setting for the DAC 402 in the charge pump 208. This information is also used to calculate coefficients for the pre-distortion filter 222.

[0053] During execution of the gain calibration algorithm, the gain calibration algorithm configures the frequency synthesizer 200. For example, the loop filter 212 is configured so that a first capacitor 404 is shorted to the common mode voltage 302 (using a switch or other suitable mechanism). Also, in one embodiment, the current supplied to the charge pump 208 in the phase-locked-loop 206 is selectable by a three-bit DAC 402. The phase detector 208 in the phase-locked-loop 206 includes UP and DOWN outputs, which are overridden so that that charge pump current is either positive or negative. From the three-bit value for the charge pump 208 and by overriding the UP and DOWN outputs of the phase detector 208, the charge pump 208 is configured as a four-bit, sign+magnitude current-mode DAC.

[0054] At this point, the analog input voltage to the voltage-controlled oscillator 214 is set by the charge pump DAC current into a resistor 406 in the loop filter 212, which controls the frequency of the oscillator 214. The analog input voltage of the oscillator 214 may be determined using the formula:

$$V_{CM} + DAC_{SETTING} I_{LSB} R_1$$

where VCM is the common mode voltage 302 in the center of the analog tuning range of the oscillator 214, DAC_{SETTING} is the digital DAC input, I_{LSB} is the LSB size of the charge pump DAC, and R₁ is the loop filter resistor 406. On average, the output
 5 frequency of the oscillator 214 may be determined using the formula:

$$f_{OUT} = f_0 + DAC_{SETTING} (I_{LSB} R_1 K_{VCO})$$

where f₀ is the output frequency of the oscillator 214 with the analog input voltage at VCM 302 for the saved capacitor select
 10 setting, and K_{VCO} represents the gain of the oscillator 214.

[0055] In one embodiment, the gain calibration algorithm performs the following steps:

(1) Set the desired frequency to $f_{DESIRED} = f_{CHAN} - \Delta f$, forcing the average output frequency to $f_{CHAN} - \Delta f$, where f_{CHAN} is
 15 the channel frequency, and Δf is a frequency value chosen to make a good two-point linear approximation to the loop gain of the phase-locked-loop 206.

(2) After the loop settles, save the average charge pump DAC input value as DAC_{NEG}. Thus,

20
$$f_{CHAN} - \Delta f = f_0 - DAC_{NEG} (I_{LSB} R_1 K_{VCO}) .$$

(3) Set the desired frequency to $f_{\text{DESIRED}} = f_{\text{CHAN}} + \Delta f$, forcing the average output frequency to $f_{\text{CHAN}} + \Delta f$.

(4) After the loop settles, save the average charge pump DAC input value as DAC_{POS} . Thus,

$$f_{\text{CHAN}} + \Delta f = f_0 + \text{DAC}_{\text{POS}}(I_{\text{LSB}} R_1 K_{\text{VCO}}).$$

(5) Calculate $\Delta \text{DAC} = \text{DAC}_{\text{POS}} - \text{DAC}_{\text{NEG}}$, where

$$\Delta \text{DAC} = \text{DAC}_{\text{POS}} - \text{DAC}_{\text{NEG}} = \frac{2\Delta f}{I_{\text{LSB}} R_1 K_{\text{VCO}}}.$$

(6) The approximate unity gain bandwidth of the phase-locked-loop may be determined using the formula:

$$\omega_{\text{LOOP}} = \frac{I_p K_{\text{VCO}} R_1 C_1}{2\pi(C_1 + C_2)N},$$

where I_p represents the current through the phase detector/charge pump 208, and N represents the scale by which the divider 216 divides the output signal 204.

(7) Using the ΔDAC and ω_{LOOP} values, given a desired loop gain $\omega_{\text{LOOP_DESIRED}}$, a corresponding ideal DAC setting $\text{DAC}_{\text{IDEAL}}$ can be determined as follows:

$$\text{DAC}_{\text{IDEAL}} = \frac{\Delta \text{DAC} \omega_{\text{LOOP_DESIRED}} 2\pi(C_1 + C_2)N}{2\Delta f C_1}.$$

(8) In one embodiment, a 3-bit DAC 402 is used in the charge pump 208. As a result, the calculated $\text{DAC}_{\text{IDEAL}}$ value for a desired loop gain may not be precisely set. Therefore, $\text{DAC}_{\text{IDEAL}}$ may be rounded down to $\text{DAC}_{\text{ACTUAL}}$, which is the 3-bit DAC setting

once the phase-locked-loop 206 is configured as a standard phase-locked-loop 206. This allows an actual loop gain close to the desired loop gain.

(9) The error between the actual loop gain (based on the actual 3-bit charge pump DAC) and an ideal charge pump current is calculated. This error value is used later to calculate coefficients for the pre-distortion filter 222. Thus,

$$\omega_{\text{LOOP_ACTUAL}} = \frac{\text{DAC}_{\text{ACTUAL}}}{\text{DAC}_{\text{IDEAL}}} \omega_{\text{LOOP_IDEAL}} .$$

[0056] A resistor-capacitor (RC) tuner algorithm may also be executed by the frequency synthesizer 200. In a particular embodiment, the RC tuner algorithm is executed concurrently with the gain calibration algorithm. Also, in a particular embodiment, separate tuner algorithms could be executed for the metal capacitor 404 (which may represent a small loop filter capacitor) and for a MOS capacitor 408 (which may represent a large loop filter capacitor). Actual values for ω_z (the loop filter zero) and ω_{p2} (the loop filter pole), ω_{z_ACTUAL} and ω_{p2_ACTUAL} , can be calculated and expressed as:

$$\omega_{z_ACTUAL} = \omega_{z_NOMINAL} \omega_{z_ERROR}$$

$$\omega_{p2_ACTUAL} = \omega_{p2_NOMINAL} \omega_{p2_ERROR} .$$

where $\omega_{z_NOMINAL}$ and $\omega_{p2_NOMINAL}$ represent the estimated loop filter

zero and loop filter pole, and ω_{Z_ERROR} and ω_{P2_ERROR} represent the error calculated above.

[0057] After the capacitor select, gain calibration, and RC tuner algorithms have been executed, the frequency synthesizer 200 may be configured as a Frac-N frequency synthesizer having a standard phase-locked-loop with the charge pump DAC 402 set to DAC_{ACTUAL} . The loop gain control reduces settling time and noise variation.

[0058] In one embodiment, the transfer function from the input of the Delta-Sigma modulator 218 to the output of the phase-locked-loop 206 is:

$$H_{PLL}(s) \cong \frac{f_{REF}(1 + \frac{s}{\omega_z})}{1 + \frac{s}{\omega_z} + \frac{s^2}{\omega_{LOOP}\omega_z} + \frac{s^3}{\omega_{P2}\omega_{LOOP}\omega_z}} .$$

[0059] To compensate for this response of the phase-locked-loop 206, the frequency response of the pre-distortion filter 222 may approximate the inverse of the phase-locked-loop's response. By using the transform $s \Leftrightarrow f_{REF}(1 - Z^{-1})$, the transfer function of the desired pre-distortion filter 222 may be determined using the formula:

$$H_{PRE}(Z) = \frac{1 + B_1(1 - Z^{-1}) + B_2(1 - Z^{-1})^2 + B_3(1 - Z^{-1})^3}{1 + A_1(1 - Z^{-1})}$$

where:

$$B_1 = \frac{f_{REF}}{\omega_z} B_2 = \frac{f_{REF}^2}{\omega_{LOOP} \omega_z} B_3 = \frac{f_{REF}^3}{\omega_{P2} \omega_{LOOP} \omega_z} A_1 = \frac{f_{REF}}{\omega_z} .$$

Using the calculated values for ω_{LOOP_ACTUAL} , ω_{Z_ACTUAL} , and ω_{P2_ACTUAL} ,
5 the coefficient values in this formula may be calculated. These
coefficient values may then be used in the pre-distortion filter
222, which filters the input signal 202 according to the
coefficients. In one embodiment, the filter coefficients may be
updated in the pre-distortion filter 222 during settling of the
10 phase-locked-loop 206 before data is transmitted, which may avoid
transients in the digital filters 220, 222.

[0060] In other embodiments, compensation for the loop gain
and the loop filter variation could be done using a higher
resolution charge-pump DAC 402 and switches in the loop filter
15 212. These could be used to adjust the component values of the
loop filter 212.

[0061] In a particular embodiment, the frequency synthesizer
200 may be implemented in 0.25 μm CMOS. In this embodiment, the
frequency synthesizer 200 could use approximately 35 mA and
20 occupy approximately 4 mm^2 die area. In this embodiment of the
frequency synthesizer 200, the time for the various algorithms to
be executed and for the output signal 204 to settle may take
approximately 140 μs .

[0062] Although FIGURE 4 illustrates one example of a gain calibration circuit 400, various changes may be made to FIGURE 4. For example, other or additional components could be used in the gain calibration circuit 400.

5 [0063] FIGURE 5 illustrates an example method 500 for digital pre-distortion according to one embodiment of this disclosure. The method 500 may be described with respect to the frequency synthesizer 200 of FIGURE 2. The method 500 could be used by any other suitable frequency synthesizer.

10 [0064] The frequency synthesizer 200 selects a capacitor setting for a voltage-controlled oscillator 214 at step 502. This may include, for example, the controller 224 configuring the frequency synthesizer 200 as a frequency-locked loop. This may also include the controller 224 allowing the capacitor select
15 circuit 300 to operate and identify a capacitor setting that causes the estimated frequency 312 to equal or approximately equal the desired frequency 316.

[0065] The frequency synthesizer 200 estimates the gain introduced by the phase-locked-loop 206 at step 504. This may
20 include, for example, the controller 224 configuring the frequency synthesizer 200 as a frequency-locked loop. As particular examples, this may include the controller 224 shorting the capacitor 404 in the loop filter 212 to the common mode

voltage 302 and overriding the UP and DOWN outputs of the phase detector 208. This may also include the controller 224 allowing the gain calibration loop 300 to operate and identify the gain using the results produced by the gain calibration circuit 400.

5 [0066] The frequency synthesizer 200 estimates the response of the loop filter 212 at step 506. This may include, for example, the frequency synthesizer 200 using the formulas above to identify values for ω_{Z_ACTUAL} and ω_{P2_ACTUAL} .

[0067] The frequency synthesizer 200 and controller 224
10 identify coefficients for the pre-distortion filter 222 at step 508. This may include, for example, the frequency synthesizer 200 identifying the transfer function of the frequency synthesizer 200. This may also include the frequency synthesizer 200 identifying the inverse of this transfer function to identify
15 another transfer function that is associated with the desired pre-distortion filter 222. This may further include the frequency synthesizer 200 identifying the coefficient values using the second transfer function. In addition, this may include the controller 224 updating the pre-distortion filter 222
20 with the new coefficient values.

[0068] The frequency synthesizer 200 allows its output to settle at step 510. This may include, for example, the frequency synthesizer 200 waiting for a specified period of time. During

this time, the pre-distortion filter 222 may settle and begin operating with its new coefficient values. The frequency synthesizer 200 transmits data at step 512. This may include, for example, the frequency synthesizer 200 filtering an input
5 signal 202 using the new settings in the pre-distortion filter 222.

[0069] Although FIGURE 5 illustrates one example of a method 500 for digital pre-distortion compensation, various changes may be made to FIGURE 5. For example, additional factors could be
10 used to identify coefficient values for the pre-distortion filter 222.

[0070] While this disclosure has described certain embodiments and generally associated methods, alterations and permutations of these embodiments and methods will be apparent to those skilled
15 in the art. Accordingly, the above description of example embodiments does not define or constrain this disclosure. Other changes, substitutions, and alterations are also possible without departing from the spirit and scope of this disclosure, as defined by the following claims.